Fault-Tolerant Adder and Multiplier Designs using Bio-Inspired Approaches

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Abstract

Adders and multipliers stand as vital digital circuit components in the realm of space and mission-critical applications. These applications are often exposed to harsh environmental conditions, encompassing radiation and high-temperature extremes. Unfortunately, the operation of these systems can be failed by the occurrence of soft errors, such as single event upsets (SEUs) and single event transients (SETs) within digital circuits. The genesis of these soft errors can be attributed to the impact of high-energy particles like gamma rays and alpha rays on electronic devices. In specific instances, the incidence of SETs within adders and multipliers can introduce erroneous values into the sequential logic unit, leading to SEUs. Left unaddressed, these soft errors have the potential to cause data processing inaccuracies and system malfunctions.To safeguard against such vulnerabilities, the integration of fault-tolerant techniques becomes indispensable within adder and multiplier circuits. Traditional approaches, such as Triple Modular Redundancy, Dual Modular Redundancy, and N-Modular Redundancy, have served as the better solutions for implementing fault tolerance. However, these conventional techniques exhibit limitations: self-adaptability and hardware overhead, a concern that increases the complexity of circuit as input size of the circuit escalates.

Recent explorations in bio-inspired electronics have yielded innovative approaches. Researchers have succeeded in developing compatible hardware architectures for diverse circuits, using the principles of bio-inspired design in conjunction with reconfigurable computing. Bio-inspired electronics inherently possess the quality of self-adaptability. This motives to design the fault-tolerant hardware design through a bio-inspired paradigm. These works were designed using Dynamic Partial Reconfiguration (DPR) and Virtual Reconfiguration Circuit (VRC) mechanisms. Notably, VRC implementation has emerged as superior, owing to its versatility across a wide array of reconfigurable devices, in contrast to the somewhat limited scope of DPR. Yet, shortcomings persist in some prior works. Notably, segments of these projects, such as the utilization of evolutionary algorithms for bitstream generation, have been externally implemented, either on personal computers (PCs) or system-on-chip (SoC) devices. Such extrinsic or hybrid implementations have adversely affected error recovery performance. Moreover, the implementation of VRC necessitates increased hardware resources, and scalability concerns as the hardware's scale expands.

In response to these challenges, our research introduces a novel paradigm: self-healing designs for adders and multipliers. In our work, we have achieved complete implementation of the architecture for these circuits on a single field-programmable gate array (FPGA), resulting in a significant enhancement of error recovery rates. This form of implementation is referred to as intrinsic. We have further proposed an optimized VRC-based circuit for adders and multipliers, featuring a streamlined bitstream. This design innovation effectively surmounts scalability issues and reduces hardware complexity. Within our work, error detection has been identified through a reference unit, and error recovery has been executed via a bitstream generation unit. Our proposed approach yields a noteworthy reduction of approximately 50% to 60% when compared to existing methodologies.